Near Void-Free Assembly Development of Flip Chip Using No-Flow Underfill

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***Abstract*—The advanced flip-chip-in-package (FCIP) process technology, using no-flow underfill material for high I/O density (over 3000 I/O) and fine-pitch (down to 150 μm) interconnect applications, presents challenges for flip chip processing because underfill void formation during reflow drives interconnect yield down and degrades reliability. In spite of such challenges, a high yield, reliable assembly process ($> 99.99\%$) has been achieved using commercial no-flow underfill material with a high I/O, fine-pitch FCIP. This has been obtained using design of experiments with physical interpretation techniques. Statistical analysis determined what assembly conditions should be used in order to achieve robust interconnects without disrupting the FCIP interconnect structure. However, the resulting high yield process had the side effect of causing a large number of voids in the FCIP assemblies. Parametric studies were conducted to develop assembly process conditions that would minimize the number of voids in the FCIP induced by thermal effects. This work has resulted in a significant reduction in the number of underfill voids. This paper presents systematic studies into yield characterization, void formation characterization, and void reduction through the use of structured experimentation which was designed to improve assembly yield and to minimize the number of voids, respectively, in FCIP assemblies.**

***Index Terms*—Assembly yield, fine pitch, flip chip, high I/O density, no-flow underfill, reliability, void formation.**

I. Introduction

THE advanced electrical, thermal, and form fact performance of flip-chip-in-package (FCIP) technology enables it to be widely used in high-performance device packaging solutions such as microprocessors, graphic devices, and high-speed memory applications. The assembly processes can be established using advanced materials systems such as underfill materials, which help to mitigate the effects of large coefficient of thermal expansion (CTE) mismatch between silicon die and organic substrate. The conventional material is capillary flow underfill; a more recently developed material is a no-flow underfill containing fluxing agents. The flip chip assembly process using no-flow underfill can save process time and cost compared to conventional capillary flow underfill process because it has simple process steps. The no-flow underfill materials are deposited onto the substrate before a chip is placed. Next, the silicon chip is placed on the substrate, causing squeezing flow of the underfill material. Then, both metallurgical solder interconnects and underfill curing are simultaneously achieved during a single reflow process. The process comparison between the flip chip assembly using conventional underfill and no-flow underfill materials are illustrated in Fig. 1 [1], [2]. However, the feasible assembly process window is limited for high yield and high reliability flip chip assembly using no-flow underfill material.

Recently, a full area-array assembly process has been reported, describing a no-flow underfill material for FCIP interconnects that use high-lead solder bumps (Pb/Sn-90/10) and eutectic lead–tin (Pb/Sn–37/63) solder paste; this was used for a flip chip device with high I/O density over 3000 I/O and fine pitch down to 150 μm [3]–[5]. The systematic experiments achieved a high-speed assembly process with wide process windows, and the process was validated using a design-of-experiment (DOE) technique, but a large number of voids in the underfill material were observed, and these could cause defects such as solder bridges and solder joint cracks, possibly resulting in early failure under thermal reliability test [6]–[10]. In particular, the voids formed adjacent solder bumps, which can be critical defects for reliability. Typical underfill voiding among solder joints in flip chip assemblies that use no-flow underfill material is shown in Fig. 2(a) and (b) by an cross-sectional view of optical micrograph. A C-mode scanning acoustic microscopy (C-SAM) in-plane view confirms multiple void areas in the underfill between the test chip and the substrate as shown in Fig. 2(c). The observed voids in these micrographs obviously could not meet the project requirement that voiding percent area should be less than 5% and that no voids exist adjacent to solder bumps.

Many researchers have thoroughly identified the causes of void formation in flip chip assemblies. Mainly the source of void formation can classified into thermally induced voids [1], [11]–[18], and nonthermally induced voids [19]. Typically, a chip placement process or the geometry effect of a test vehicle's design can cause nonthermally induced voids. Among them, our investigation focused on the thermal effects from the reflow process to explain void formation for the current large number of underfill voiding patterns. Moreover, the mechanism of underfill voiding was suggested in our past research [13]. The study explained that the source of underfill voiding was mainly the fluxing agent in no-flow underfill. The fluxing agent can be exposed to temperatures above its boiling point during the reflow

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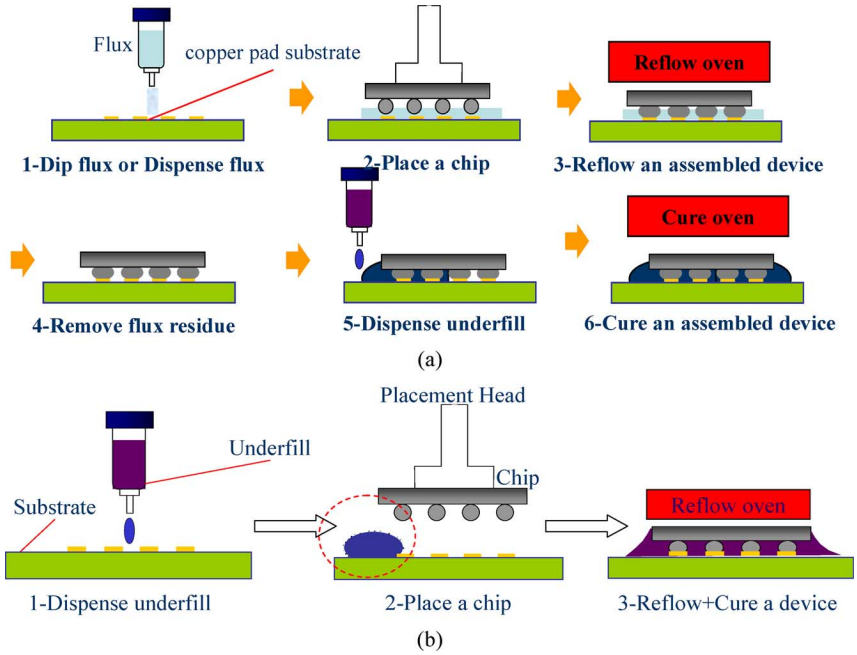

Fig. 1. Flip chip assembly process. (a) Conventional assembly process and (b) Hybrid no-flow assembly process [13].

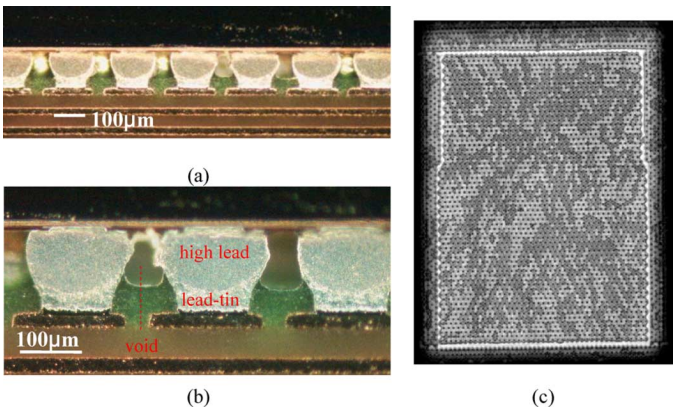

Fig. 2. Micrographs of FCIP built using no-flow underfill material under the reflow conditions of ramp rate: 2.1 °C/s, reflow time: 70 s, peak temp: 225 °C. (a) cross-sectional view of flip chip solders joints (magnification: 100 ×). (b) Cross-sectional view of flip chip solders joints (magnification: 200 ×). (c) C-SAM analysis [13].

process for solder melting and underfill curing. Thus, the chemical reactions induced underfill voiding. Eventually, a general void formation mechanism was suggested to explain the current large amount of no-flow underfill voiding with a high I/O and fine pitch flip chip application.

With that void formation mechanism, this study investigated the effect of reflow process conditions on the underfill void formation in the flip chip assembly; the goal was to validate the no-flow underfill mechanism using experimental techniques. This validation can determine the best assembly conditions to minimize the number of voids for robust flip chip interconnects. Thus, this can provide a design guideline to achieve a near void-free and high, stable yield assembly process using no-flow underfill materials with a high I/O counts and fine-pitch devices. Consequently, the assembly process might easily accomplish high reliability performance.

TABLE I
MATERIAL PROPERTIES OF NO-FLOW UNDERFILL

(a) Underfill A

Material property	Value
Glass transition temperature (Tg)	81 °C
Viscosity @ 25°C	3,100 cp
Flexural modulus	2.6 GPa
Coefficient of thermal expansion below Tg	190 ppm/°C
Cure condition	a standard SMT reflow incorporating at 150-170°C dwell prior to ramp up to reflow temperature

(b) Underfill B

Material property	Value
Glass transition temperature (Tg)	100 °C
Viscosity @ 25°C	1,500 cp
Flexural modulus	3.0 GPa
Coefficient of thermal expansion below Tg	215 ppm/°C
Cure condition	a standard SMT reflow incorporating at 150-170°C dwell prior to ramp up to reflow temperature

II. EXPERIMENT

A series of experiments, outlined in Fig. 3, were performed to establish the foundation for a high yield no-flow underfill assembly process using simple structured test vehicles and a low-cost flip chip test vehicle. The simple structured test vehicles were used to determine wetting conditions for high-lead solder bumps and plated lead–tin pad interconnect systems.

TABLE II
DESIGN MATRIX OF DOE FOR YIELD CHARACTERIZATION STUDY IN THE FIRST ROUND

Material	Levels	Initial ramp rate	Soak time (140 ~ 170 °C)	Time above liquidus	Peak temperature
Underfill A (2 replicates)	Level 1	2.1 °C/s	0sec	70sec	225 °C
	Level 2	2.3 °C/s	50sec	80sec	235°C
Underfill B (2 replicates)	Level 1	1.1 °C/s	50sec	95sec	225 °C
	Level 2	1.3 °C/s	60sec	115sec	235°C

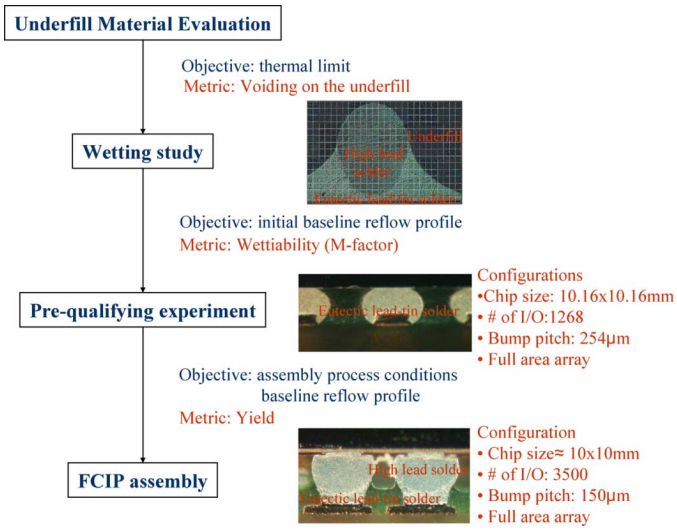

Fig. 3. Assembly process development procedures.

TABLE III
CONFIGURATION OF TEST VEHICLES USED IN THE EXPERIMENTS

Experiment	Category	
Assembly yield characterization	Bump material	97Pb-3Sn
	Die size(mm)	< 10 x 10
	Bump count	3000 >
	Bump pitch	< 200μm
	Bump layout	Full area
	Surface finish	36Pb-63Sn
Void formation characterization	Die material	Glass cover
	Bump count	3000 >
	Bump pitch	< 200μm
	Bump layout	Full area
	Surface finish	36Pb-63Sn
Void reduction study	Die material	Silicon
	Bond pad	36Pb-63Sn
	Bump material	97Pb-3Sn
	Die size(mm)	< 10 x 10
	Bump count	3000 >
	Bump pitch	< 200μm
	Bump layout	Full area

These wetting conditions were used as the baseline of a prequalifying experiment. The prequalifying experiment used a low-cost FA10–4 flip chip test vehicle to validate the process prior to assembling the full area array, high I/O, fine-pitch flip chip in package (FCIP) architectures. The validated assembly process was further optimized to achieve robust interconnection by investigating the effect of reflow parameters on electrical yield using a high I/O, fine-pitch FCIP test vehicle. Eventually, a high-yield assembly process with wide variation of reflow parameters was achieved with the FCIP. On the other hand, the high-yield assembly process had a large number of voids on the FCIP device (see Fig. 2). The work was comprised of an assembly yield characterization study, a void formation characterization, and a void reduction study. Statistical analysis was used to determine the reflow process conditions required to improve the assembly's yield with a wide process window. In addition, no-flow underfill voiding was characterized with respect to reflow process conditions in order to minimize the number of voids, which can be a critical defect that affects early failure in thermal reliability. A void reduction study was performed to decrease underfill voiding; the study used a parametric characterization of reflow process conditions. The test vehicles used are summarized in Table I.

A. *Assembly Yield Characterization*

The main objective was to determine the effects of reflow parameters on assembly yield for high I/O density, fine-pitch FCIP assemblies by using statistical analysis. The DOE had four factors including ramp rate, soak time, time above liquidus, and peak temperature with two levels and two replicates as described in Table II. The baseline reflow process parameters were determined using statistical analysis in our past research [4], [5], [7]. These studies examined several commercial no-flow underfills. The materials that performed best in these previous studies were used for this study focusing on high I/O, fine-pitch FCIP. The material properties of no-flow underfill materials and the specifications of the test vehicles are summarized in Tables I and III, respectively.

Prior to the assembly process, boards were exposed to an isothermal environment at 125 °C for 3 h to drive out all moisture. This bake condition was sufficient to avoid the problem of moisture out-gassing from the boards [20], [21]. Next, a plasma pretreatment was applied to the substrate surface to promote a clean surface and to improve underfill processing. The plasma pretreatment required, first, exposure to a pure argon (Ar) plasma for 10 min to remove contamination and

TABLE IV
DOE FOR YIELD CHARACTERIZATION STUDY IN THE FIRST ROUND

(a) underfill A

Run order	Initial ramp rate	Soak time	Time above liquidus	Peak temp	Yields
1,2	1	1	1	1	Pass
3,4	2	1	2	1	Pass
5,6	1	1	2	2	Pass
7,8	2	1	1	2	Pass
9,10	2	2	1	1	Pass
11,12	1	2	2	1	Pass
13,14	1	2	1	2	Pass
15,16	2	2	2	2	Pass
Total builds	16				16 (100%)

(b) underfill B

Run order	Initial ramp rate	Soak time	Time above liquidus	Peak temp	Yields
1, 2	1	1	1	1	Pass
3, 4	2	1	2	1	Pass
5, 6	1	1	2	2	Pass
7	2	1	1	2	Fail (Short)
8	2	1	1	2	Pass
9	2	2	1	1	Pass
10	2	2	1	1	Fail (Open)
11, 12	1	2	2	1	Pass
13, 14	1	2	1	2	Pass
15, 16	2	2	2	2	Pass
Total Builds	16				14(87.5%)

to improve surface wetting. Next, the high I/O, fine-pitch flip chips were assembled using two commercial no-flow underfills as illustrated in Fig. 1(a). The applied no-flow assembly technique used the line edge dispense pattern to prevent a chip's placement from inducing voids [12], [22], [23]. Then, the assembled packages were reflowed according to a full factorial design of experiment (DOE) described in Tables IV(a) and IV(b), respectively. Statistical techniques investigated the main effect and the interactive effects of reflow parameters in order to improve the assembly yield based on electrical interconnect measurements in the first and second round yield characterization. Finally, the best process condition was validated for the stability of assembly yield in the third round using a large scale of assemblies (30 assemblies).

B. Void Formation Characterization

Prior research has indicated that the most significant effect on no-flow underfill voiding is the chemical reaction and interactions between solder melting, underfill curing, and solder wetting. The chemical reaction between melting solder and underfill curing is mainly induced by the fluxing agent. Commercial no-flow underfills typically use carboxylic acid for a fluxing agent. Carboxylic acid has a boiling point around 130 °C. As a result, the fluxing agent is exposed to temperatures above its boiling point during solder reflow conditions, potentially causing outgassing and void formation. For example, the soak temperature for some high yield process conditions is higher than the fluxing agent's boiling temperature, which may lead to void formation [13].

Specifically, the current soak temperature of a high yield assembly process might be higher than the fluxing agent's boiling point in the commercial no-flow underfill. Thus, a test vehicle, illustrated in Fig. 4 and Table III is used to investigate the effect of soak temperature on underfill voiding using the no-flow underfill A, which was selected as a baseline material due to high performance in assembly yield characterization. Two different temperature ranges were considered in this study. This experimental study examined the range from 140 °C to 170 °C and from 120 °C to 130 °C to investigate the effect of soak temperature on underfill voiding. The former was used for the high-yield

TABLE V
REFLOW CONDITIONS FOR VOID REDUCTION STUDY

Condition	(1)	(2)	(3)	(4)
Initial ramp rate	1.3°C/s	1.3°C/s	1.3°C/s	1.3°C/s
Soak temp	140~170 °C	120~130 °C	120~130 °C	120~130 °C
Soak time	50 sec	90 sec	120 sec	150 sec
Time above liquidus	70 sec	70 sec	70 sec	70 sec
Peak temp	225 °C	225 °C	225 °C	225 °C

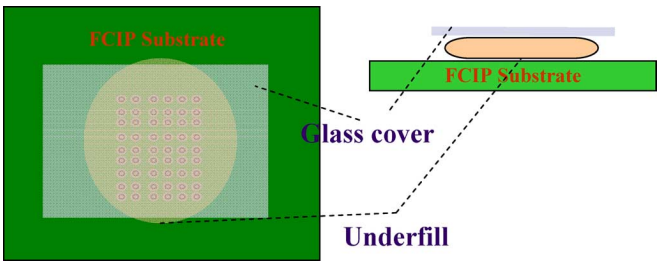

Fig. 4. Configuration of test vehicle for void characterization study.

assembly process and the latter was selected for void characterization, respectively. The lower soak temperature was expected to enable the fluxing agent to remove oxidation and to participate in underfill curing below its boiling temperature.

The prebaking and pretreatment used in the previous yield characterization were consistently applied to void characterization, respectively. Next, underfill was dispensed on the FCIP substrate and a glass cover die was placed on the underfill deposited substrate. The glass cover the voiding to be inspected without C-SAM or destructive analysis right after a reflow process. Then assembled test vehicles were reflowed at two levels of soak temperatures conditions such as from 140 °C to 170 °C and from 120 °C to 130 °C. The other parameters were determined according to the conditions of minimum amount of underfill outgassing with margin of assembly yield that were found in past studies [4], [5], [7]. On the experimental results, the ramp rate was 1.3 °C/s, soak time was 90 s, the time above liquidus was 70 s, and the peak temperature was 225 °C. Finally, the underfill voiding was inspected using an optical microscope.

C. Void Reduction Study

The objective of this void reduction study is to validate the result of void characterization using high I/O, fine-pitch FCIP packages (see Table III). In addition, this study determines the reflow process parameters to use in order to minimize the amount of underfill voiding for commercial no-flow underfill A. This is accomplished by modifying the soak temperature and soak time as described in Table V. The pretreatments used in previous studies were applied to the void reduction study. Next, underfill was dispensed on the FCIP substrate and a silicon die was placed on the underfill deposited substrate. Then assembled test vehicles were reflowed at four different assembly process conditions as shown in Table V. Afterwards, each test condition was scanned using C-SAM. The amount of underfill voiding was defined as the void percent area. It presented the total voids area of total flip chip device area, as obtained using an image process technique [4], [7], [24]. The low void percent area can be meaningful in the case where 100% electrical interconnects are achieved.

III. RESULTS AND DISCUSSION

A. Assembly Yield Characterization

The assembly yield characterization evaluated two commercial underfill materials such as underfill A and underfill B. The yield performance of both materials is summarized in Table VII. In the first round, a high-yield assembly process was accomplished with high I/O, fine-pitch flip chip packages using underfill A as described in Table IV(a). In contrast, underfill B could not achieve a high-yield assembly process with a DOE technique as described in Table IV(b). Thus, the statistical analysis determined the optimal reflow parameters, enabling a high yield assembly process. From the ANOVA analysis with 95% confidence interval, the ramp rate and the time above liquidus (reflow time) could affect the assembly yield (see Table VI). However, 0.149 p indicated that both factors could be significant as presented in Table VI. On the main effect and interactive effects of reflow parameters, assembly yield could be increased with low ramp rate regardless of time above liquidus as shown in Fig. 5. With 1.1 °C/s ramp rate and 95 s time above liquidus in level 1, a two-level DOE of four factors with two replicates was suggested for the second round yield characterization of underfill B in order to improve assembly yield and potentially voiding characteristics as described in Table VIII. Consequently, the second round achieved a high-yield assembly process, since 16 assembled parts achieved electrical interconnection. Then, the stability of the high-yield process was validated in the third round with a large number of assemblies using underfill A and B, respectively, as described in Table IX. The process conditions were selected intuitively for high assembly and minimum amount of underfill voiding, since both materials have wide process windows on the second round yield characterization. In the case of underfill A, it was found that the feasible assembly process conditions enabled a high yield, reliable assembly process with wide process windows. In contrast, three yield losses were observed in 30 assemblies built using underfill B. From the view of mass production, underfill B could not be a

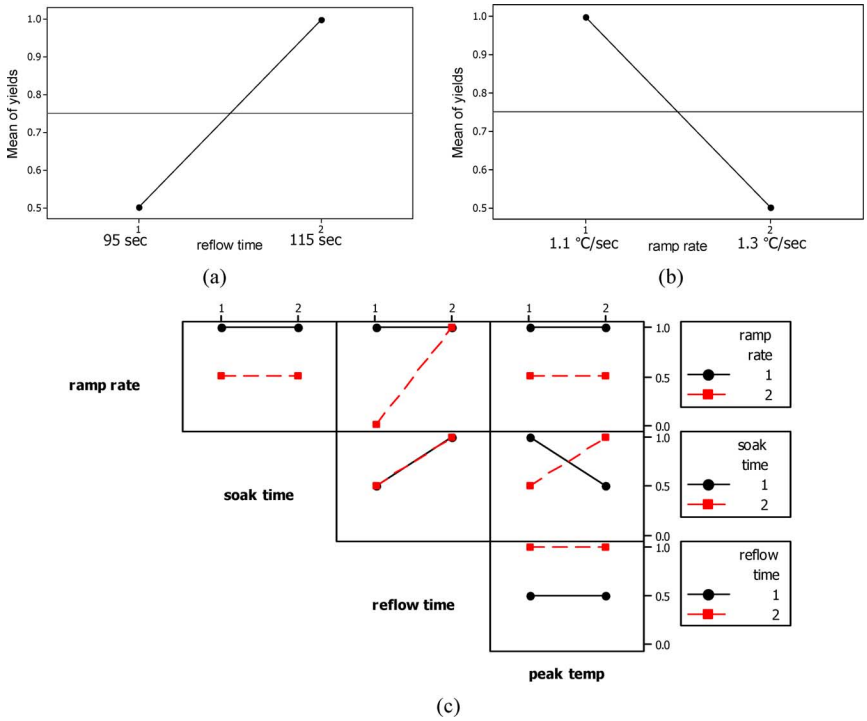

Fig. 5. Main effect plots (a) reflow time and (b) ramp rate, interactive effect plot (c) reflow parameters.

TABLE VI
ANOVA: YIELD VERSUS RAMP RATE AND VERSUS REFLOW TIME

Source	DF	SS	MS	F	P
Ramp rate Reflow time	1	1.000	1.000	2.33	0.149
Error	14	6.000	0.429		
Total	15	7.000			

TABLE VII
ASSEMBLY YIELD CHARACTERIZATION OVERVIEW

	Underfill A		Underfill B	
parts	assembled	yielded	assembled	yielded
First	16	16	16	14
Second	0	0	16	16
Third	31	31	30	27
Total	47	47	62	57

TABLE VIII
DESIGN MATRIX OF DOE FOR YIELD CHARACTERIZATION STUDY IN THE SECOND ROUND

Levels/Factors	Initial ramp rate	Soak time (140 ~ 165 °C)	Time above liquidus	Peak temperature
Level 1	0.9 °C/s	60sec	95 sec	210 °C
Level 2	1.1 °C/s	70sec	105 sec	225 °C

TABLE IX
PROCESS CONDITIONS FOR YIELD CHARACTERIZATION STUDY IN THE THIRD ROUND

Material	Initial ramp rate	Soak time	Time Above liquidus	Peak temperature
Underfill A	2.1 °C/s	50sec (140 ~ 170 °C)	70 sec	225 °C
Underfill B	0.9 °C/s	60sec (140 ~ 165 °C)	95 sec	225 °C

good candidate due to the inconsistent performance of assembly yield.

B. Void Formation Characterization

The effect of soak temperature on void formation was investigated using commercial no-flow underfill A, since the material achieved a high, stable yield assembly process in the previous study. The underfill did not exhibit underfill voiding as shown in Fig. 6(b) at low soak temperature range from 120 °C to 130 °C. On the other hand, voids were observed with the high soak temperature as shown in Fig. 6(a). Therefore, the void formation

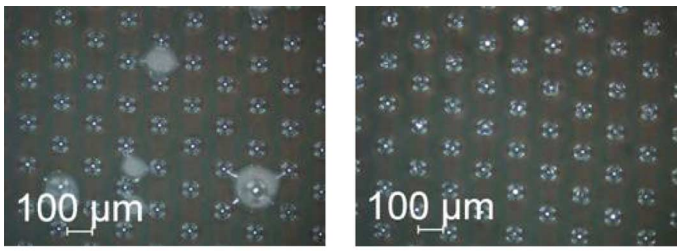

Fig. 6. Configuration of test vehicle for void characterization study. (a) 140 °C –170 °C soak temperature and (b)120 °C –130 °C soak temperature.

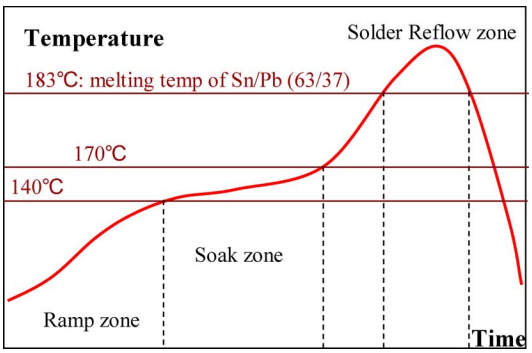

Fig. 7. Typical no-flow underfill reflow profile.

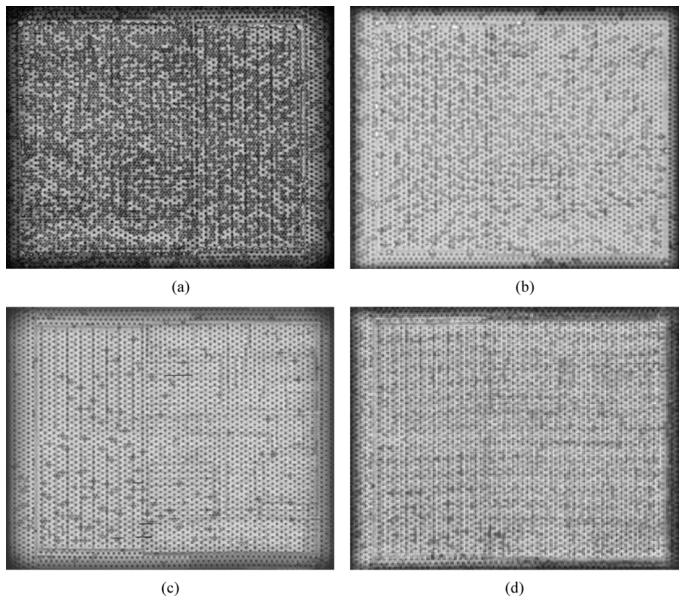

Fig. 8. Typical micrographs of a FCIP test vehicle built using no-flow underfill, Void percent area (a) 64.7%, (b) 32.2%, (c) 19.8%, and (d) 7.1%.

characterization found that the soak temperature has strong effect on the underfill voiding with the high I/O, fine-pitch flip chip on substrate.

Indeed, the most significant effect on no-flow underfill voiding was reported as the chemical reaction between solder melting and underfill curing in the FCIP [13], [19]. The chemical reaction between solder melting and underfill curing is mainly induced by the fluxing agent. Actually, the fluxing agent will reduce the oxides on solder bumps/pads, reduce surface tension of molten solder, protect the solder joint from re-oxidation, and help clean some types of surface contaminants, promoting good solder wetting conditions. In general, the fluxing agent typically is activated from 140 °C to 170 °C, called the soak temperature as shown in Fig. 7. This activation temperature enables the fluxing agent of no-flow underfill to remove oxidation and to participate in underfill curing. Actually, the achieved high-yield assembly process used a range temperature from 140 °C to 170 °C for the soak temperature with high I/O, fine-pitch FCIP using no-flow underfill. This temperature range might be higher than the boiling point of the flux agent. The no-flow underfill typically uses carboxylic acetic acid for a fluxing agent. Carboxylic acid typically boils at around 130 °C, which can be influenced by material property such as acidity [25]. As a result, the fluxing agent is exposed to temperatures above its boiling point, causing possible outgassing voids. Specifically, the current soak temperature of the high-yield assembly process might be higher than fluxing agent's boiling temperature in the no-flow underfill material used [13]. As a result, the fluxing agent is exposed to temperatures above its boiling temperature, causing outgassing voids [13] with high soak temperatures from 140 °C to 170 °C. In contrast, low soak temperatures, from 120 °C to 130 °C, enable the fluxing agent to remove oxidation around solders at stable temperature range below its boiling temperature. This understanding provides an idea of how the long soak time may reduce underfill voiding since the fluxing agents can remove oxidation around solders and then restore for underfill curing at stable soak temperature [13]. Thus, a void reduction study will investigate the effect of soak temperature and soak time on underfill voiding, using a parametric study with real package assemblies in void reduction study.

C. Void Reduction Study

In general, low soak temperature and long soak time can minimize the percent void area. The underfill voiding could be controlled with changes to soak temperature and soak time on the void formation characterization by using a quantitative analysis. Consequently, this study found the limit of reflow process, which achieved the high yield and minimum the number of voids as shown in Fig. 8. The dark gray and white of Fig. 8 presents the underfill voiding in the micrograph of C-SAM. Image process techniques were applied to detect voids and to calculate the void percent area. The results have a precision by mapping detected voids with actual voids on the micrographs of planar sectional view [4], [5], [7], [24], [26].

Namely, the new suggested low soak temperature from 120 °C to 130 °C dramatically reduced the percent void area. The percent area was reduced from 64.7% to 32.2% by modifying only the soak temperature range. Besides, the long soak time can almost eliminate underfill voiding, reducing it to 7.0%. With long soak time at low soak temperature, the flux agent could remove oxidation and participate in underfill curing at stable condition prior to the peak temperature zone. Consequently, the number of voids could be minimized with understanding of voiding mechanism.

IV. Conclusion

Advanced FCIP process technology using no-flow underfill material for high I/O density and fine-pitch interconnect applications presents challenges for no-flow underfill flip chip processing because underfill void formation during reflow drives interconnect yield down and degrades reliability performance. In this paper, parametric studies were conducted to develop assembly process conditions that would minimize underfill voids in the FCIP assemblies. This work has resulted in a significant reduction in the number of underfill voids.

The yield characterization study investigated the main effect on assembly yield of reflow parameters such as ramp rate, soak time, time above liquidus, and peak temperature. For the commercial no-flow underfills studied, the yield could be increased with lower ramp rates and longer time above liquidus. The stability of the assembly process for both commercial no-flow underfills studied was validated. In general, the assembly yield might be affected by the mechanical property such as viscosity. With low viscosity, a chip could be shifted causing yield losses. However, these assemblies had excessive underfill voiding. The mechanism of yield loss can be identified with substantial studies.

The void characterization investigated the effect of reflow soak parameters on underfill voiding. With a lower soak temperature, 120 °C to 130 °C, the flux agent promotes fluxing action to remove surface oxides and to participate in underfill curing reacting back into the final material structure. This soak temperature range eliminated the underfill voiding in the simple structured test vehicles, indicating that this low soak temperature can be a potential way to minimize the number of underfill voids in the FCIP assemblies.

The void reduction study investigated the effect of soak temperature and soak time on underfill voiding in FCIP test vehicles by using a parametric variation of soak time and soak temperature. The result was a significant reduction in void percent area from 64% to 7%. The optimal conditions suggest the lower soak temperature and longer soak time tend to minimize voids. The optimal conditions could be achieved with the low soak temperature and long soak time for minimal number of voids. Therefore, the findings in this study provide the process design guideline for a highly reliable assembly process using no-flow underfill with high I/O and fine-pitch flip chip device. Furthermore, a void free flip chip assembly process can be achieved using no-flow underfills in order to achieve long-term thermomechanical reliability on the results of these studies.

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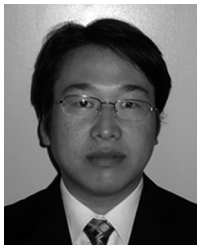

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